CLAIMS

What is claimed is:

1. A method of downconverting a signal and rejecting an image, comprising:

providing a first, second, third, fourth and fifth signal, wherein the first signal has a frequency F, the second signal has a frequency F/N, the third signal has a frequency F/N and is phase shifted 90° with respect the second signal; the fourth signal has a frequency F/NM, and the fifth signal has a frequency F/NM and is phase shifted 90° from the fourth signal;

mixing the first signal with an input signal to produce a first mixer output signal;

splitting the first mixer output signal to produce a first splitter output signal and a second splitter output signal;

mixing the first splitter output signal with the second signal to produce a second mixer output signal;

mixing the second splitter output signal with the third signal to produce a third mixer output signal;

mixing the second mixer output signal with the fourth signal to produce a fourth mixer output signal;

mixing the third mixer output signal with the fifth signal to produce a fifth mixer output signal; and

combining the fourth mixer output signal and the fifth mixer output signal to produce a combiner output signal.

2. The method of Claim 1, wherein mixing the first splitter output signal with the second signal to produce a second mixer output signal further comprises low-pass filtering.

3. The method of Claim 2, wherein mixing the second splitter output signal with the third signal to produce a third mixer output signal further comprises low-pass filtering.

4. The method of Claim 1, wherein N and M are integers greater than 1.

5. The method of Claim 4, wherein N and M are each multiples of 2.

6. The method of Claim 3, wherein providing the second, third, fourth, and fifth signals comprises digitally dividing the first signal.

7. The method of Claim 5, wherein N equals 2 and M equals 4.

8. The method of Claim 3, wherein F is a frequency in the range of 3.113 GHz to 3.545 GHz.

9. The method of Claim 8, wherein the input signal has a frequency in the range of 5.15 GHz to 5.825 GHz.

10. The method of Claim 9, wherein the combiner output signal has a frequency of 90 MHz.

11. A method of upconverting a signal, and rejecting an image, comprising:

providing a first, second, third, fourth and fifth signal, wherein the first signal has a frequency F, the second signal has a frequency F/N, the third signal has a frequency F/N and is phase shifted 90° with respect the second signal; the fourth signal has a frequency F/NM, and the fifth signal has a frequency F/NM and is phase shifted 90° from the fourth signal;

splitting an input signal to produce a first splitter output signal a and second splitter output signal;

mixing the first splitter output signal with the fifth signal to produce a first mixer output signal;

mixing the second splitter output signal with the fourth signal to produce a second mixer output signal;

high-pass filtering the first mixer output signal and the second mixer output signal to produce, respectively a first filter output and a second filter output;

mixing the first filter output with the third signal to produce a third mixer output signal;

mixing the second filter output with the second signal to produce a fourth mixer output signal;

combining the third mixer output signal and the fourth mixer output signal to produce combiner output signal; and

mixing the combiner output signal with the first signal to produce a transmitter output signal.

12. The method of Claim 11, wherein N and M are integers greater than 1.

13. The method of Claim 12, wherein N and M are each multiples of 2.

14. The method of Claim 11, wherein providing the second, third, fourth, and fifth signals comprises digitally dividing the first signal.

15. The method of Claim 13, wherein N and M each equal 4.

16. A method of rejecting an image, comprising:

mixing an input signal with a local oscillator signal to produce a first intermediate frequency signal;

splitting the first intermediate frequency signal into a first part and a second part;

mixing the first part with a first clock signal to produce a first second-intermediate-frequency signal, and mixing the second part with a second clock signal, to produce a second second-intermediate-frequency signal;

filtering the first and second second-intermediate-frequency signals;

mixing the filtered first second-intermediate-frequency signal with a third clock signal to produce a first third-intermediate-frequency signal, and mixing the filtered second second-intermediate-frequency signal with a fourth clock signal to produce a second third-intermediate-frequency signal; and

combining the first third-intermediate-frequency signal with the second third-intermediate-frequency signal to produce an output signal;

wherein the first and second clock signals have a frequency that is less than that of the local oscillator by a factor of N, and the second clock signal is phase

shifted 90° from the first clock signal, the third and fourth clock signals have a frequency that is less than that of the local oscillator by a factor of NM, and the fourth clock signal is phase shifted 90° from the third clock signal, and N and M are integers greater than one.

17. The method of Claim 16, wherein N is a multiple of 2.

18. The method of Claim 16, wherein M is a multiple of 2.

19. The method of Claim 16, wherein N and M are each a multiple of 2.

20. The method of Claim 16, wherein the image is rejected in a receiver.

21. The method of Claim 16, wherein the image is rejected in a receiver, N and M are each a multiple of 2, and the filtering comprises low-pass filtering.

22. A method of rejecting an image, comprising:

splitting a transmit baseband signal into a first part and a second part;

mixing the first part with a first clock signal to produce a first second-intermediate-frequency signal, and mixing the second part with a second clock signal, to produce a second second-intermediate-frequency signal;

high-pass filtering the first second-intermediate-frequency signal, and high-pass filtering the second second-intermediate-frequency signal;

mixing the high-pass filtered first second-intermediate-frequency signal with a third clock signal to produce a first third-intermediate-frequency signal, and mixing the high-pass filtered second second-intermediate-frequency signal with a fourth clock signal to produce a second third-intermediate-frequency signal;

combining the first third-intermediate-frequency signal with the second third-intermediate-frequency signal to produce a combined signal; and

mixing the combined signal with a local oscillator signal to produce a transmit output signal;

wherein the first and second clock signals have a frequency that is less than that of the local oscillator by a factor of NM, and the second clock signal is phase shifted 90° from the first clock signal, the third and fourth clock signals have a frequency that is less than that of the local oscillator by a factor of N, and the fourth clock signal is phase shifted 90° from the third clock signal, and N and M are integers greater than one.

23. The method of Claim 22, wherein N and M are multiples of 2.

24. The method of claim 23, wherein the second part of the split transmit baseband signal is phase-shifted 180 degrees from the first part of the split transmit baseband signal.

25. An image rejection circuit, comprising:

a local oscillator, a first divider coupled to the local oscillator, and a second divider coupled to the first divider network;

a first mixer having a first and second input terminals, and an output terminal;

a first splitter having an input terminal coupled to the output terminal of the first mixer, and having a first and a second splitter output terminal;

a second mixer having a first input terminal coupled to the first output terminal of the first splitter, a second input terminal coupled to an in-phase output terminal of the first divider, and having an output terminal;

a third mixer having a first input terminal coupled to the second output terminal of the first splitter, a second input terminal coupled to a quadrature-phase output terminal of the first divider, and having an output terminal;

a first filter coupled to the second mixer output terminal, and a second filter coupled to the third mixer output terminal;

a fourth mixer having a first input terminal coupled to the first filter, a second input terminal coupled to an in-phase output terminal of the second divider, and having an output terminal;

a fifth mixer having a first input terminal coupled to the second filter, a second input terminal coupled to a quadrature-phase output terminal of the second divider, and having an output terminal; and

a combiner having a first input terminal coupled to the output terminal of the fourth mixer, a second input terminal coupled to the output terminal of the fifth mixer, and having an output terminal.

26. The circuit of Claim 25, wherein the in-phase and quadrature-phase output terminals of the first divider are adapted to provide signals that are phase shifted 90° from each other.

27. The circuit of Claim 26, wherein the in-phase and quadrature-phase output terminals of the first divider are adapted to provide signals that are the same frequency as each other, and that frequency is less than that of the local oscillator by a first factor which is a multiple of 2.

28. The circuit of Claim 27, wherein the in-phase and quadrature-phase output terminals of the second divider are adapted to provide signals that are the same frequency as each other, and that frequency is less than that of the local oscillator by a second factor which is a multiple of 2.

29. The circuit of Claim 28, wherein the second factor is greater than the first factor.

30. The circuit of Claim 25, wherein the first filter and the second filter are each low-pass filters.

31. The circuit of Claim 25, wherein the first input terminal of the first mixer is coupled to an input signal source.

32. The circuit of Claim 31, wherein the second input terminal of the first mixer is coupled to the local oscillator.

33. An image rejection circuit, comprising:

a local oscillator, a first divider coupled to the local oscillator, and a second divider coupled to the first divider;

a first splitter having an input terminal coupled to an input signal source, a first output terminal and a second output terminal;

a first mixer having a first input terminal coupled to the first output terminal of the first splitter, a second input terminal coupled to a second output terminal of the second divider, and an output terminal;

a first high-pass filter coupled to the output terminal of the first mixer;

a second mixer having a first input terminal coupled to the second output terminal of the first splitter, a second input terminal coupled to a first output terminal of the second divider, and an output terminal;

a second high-pass filter coupled to the output terminal of the second mixer;

a third mixer having a first input terminal coupled to first high-pass filter, a second input terminal coupled to a second output terminal of the first divider, and an output terminal;

a fourth mixer having a first input terminal coupled to the second filter, a second input terminal coupled to a first output terminal of the first divider, and having an output terminal;

a combiner having a first input terminal coupled to the output terminal of the third mixer, a second input terminal coupled to the output terminal of the fourth mixer, and an output terminal; and

a fifth mixer having a first input terminal coupled to the output terminal of the combiner, a second input terminal coupled to an output of the local oscillator, and having an output terminal.

34. The circuit of Claim 33, wherein the input terminal of the first splitter is coupled to an input signal source.

35. The circuit of Claim 33, wherein the input terminal of the first splitter is coupled to a transmit baseband signal source.

36. The circuit of Claim 33, wherein the first divider and the second divider each divide by factor wherein the factor is a multiple of 2.

37. An image rejection circuit, comprising:

a local oscillator, a first divider coupled to the local oscillator, and a second divider coupled to the local oscillator;

a first mixer having two input terminals and an output terminal;

a first splitter having an input terminal coupled to the output terminal of the first mixer, and having a first and a second splitter output terminal;

a second mixer having a first input terminal coupled to the first output terminal of the first splitter, a second input terminal coupled to an in-phase output terminal of the first divider, and having an output terminal;

a third mixer having a first input terminal coupled to the second output terminal of the first splitter, a second input terminal coupled to a quadrature-phase output terminal of first divider, and having an output terminal;

a first filter coupled to the second mixer output terminal, and a second filter coupled to the third mixer output terminal;

a fourth mixer having a first input terminal coupled to the first filter, a second input terminal coupled to an in-phase output terminal of the second divider, and having an output terminal;

a fifth mixer having a first input terminal coupled to the second filter, a second input terminal coupled to a quadrature-phase output terminal of the second divider, and having an output terminal; and

a combiner having a first input terminal coupled to the output terminal of the fourth mixer, a second input terminal coupled to the output terminal of the fifth mixer, and having an output terminal.

38. The circuit of Claim 37, wherein the first divider and the second divider each divide by factor wherein the factor is a multiple of 2.

39. An image rejection circuit, comprising:

a local oscillator, a first divider coupled to the local oscillator, and a second divider coupled to the local oscillator;

a first splitter having an input terminal coupled to an input signal source, a first output terminal and a second output terminal;

a first mixer having a first input terminal coupled to the first output terminal of the first splitter, a second input terminal coupled to a second output terminal of the second divider, and an output terminal;

a first high-pass filter coupled to the output terminal of the first mixer;

a second mixer having a first input terminal coupled to the second output terminal of the first splitter, a second input terminal coupled to a first output terminal of the second divider, and an output terminal;

a second high-pass filter coupled to the output terminal of the second mixer;

a third mixer having a first input terminal coupled to first high-pass filter, a second input terminal coupled to a second output terminal of the first divider, and an output terminal;

a fourth mixer having a first input terminal coupled to the second filter, a second input terminal coupled to a first output terminal of the first divider, and having an output terminal;

a combiner having a first input terminal coupled to the output terminal of the third mixer, a second input terminal coupled to the output terminal of the fourth mixer, and an output terminal; and

a fifth mixer having a first input terminal coupled to the output terminal of the combiner, a second input terminal coupled to an output of the local oscillator, and having an output terminal.

40. The circuit of Claim 39, wherein the first divider and the second divider each divide by factor wherein the factor is a multiple of 2.